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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SEYE, ABDOU K	

ART UNIT	PAPER NUMBER
2194	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/769,330	JAMES-ROXBY ET AL.	
	Examiner	Art Unit	
	Abdou Karim Seye	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08/27/2004, 10/10/2006,11/30/2007,03/03/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

. DETAILED ACTION

1. Claims 1-20 are pending in this application.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of

activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 14-17 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2 of U.S. Patent No. 7185309, and claims 1-6,10-16, 24 of U.S. Patent No. 7228520. Although the conflicting claims are not identical, they are not patentably distinct from each other because the examined application claims are an obvious variation of the invention claimed in U.S. Patent No. **7185309, 7228520** . See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); and In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985). In determining whether a nonstatutory basis exists for a double patenting rejection, the first question to be asked is — does any claim in the application define an invention that is anticipated by, or is merely an obvious variation of, an invention claimed in the patent? If the answer is yes, then an "obviousness-type" nonstatutory double patenting rejection may be appropriate. See MPEP 804 (II)(B)(1) Nonstatutory Double Patenting, Obvious-Type. The difference between the inventions defined by the conflicting claims is that **7228520** recites a (programming a design tool); **7185309** recites a (configuring a memory interconnection component for threads) while the instant application recites a (as design tool for interconnection of instances/threads). A person of ordinary skill in the art would

conclude that it is obvious to have a design tool for interconnection of instances/threads using an integrated circuit.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

5. Claims 8-9 and 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following terms lack antecedent basis:

(i) " said multithreading system", Claim 8.

(ii) "the system", claims 15-17.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title.

7. Claims 14-17 and 18-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

8. As per claims 14-17 are rejected under 35 U.S.C. 101 because the claim invention " a design tool" is recited in claim 14; however, it appears that the design tool would reasonably be interpreted by one of ordinary skill in the art as software, per se since the input section, first database, second database and multithread model section would reasonably be interpreted by one of ordinary skill in the art as software, per se. As such, it believed that the design tool of claim 14 is reasonably interpreted as functional descriptive material, per se, failing to be tangibly embodied or stored on a medium. Dependant claims 15-17 are also affected by this claim rejection.

9. As per claims 18-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to an apparatus claims comprising a first configure portion and a second configure portion that appear to be software modules/functions alone without claiming associated computer hardware required for storage and execution. Software alone is directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103 (a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-2, 5-8, 11-16 and 18 are rejected under 35 U.S.C. 103 (a) as unpatentable over Ma (US 20050038806) in view of Nishida et al. (US 6704914).

12. As to claim 18, Ma teaches the invention substantially as claimed including an apparatus (abstract; 104, FIG. 1) for multithread processing of messages using an integrated circuit (110; FIG. 1; paragraph 15), comprising:

a first configured portion within said integrated circuit for processing messages using a plurality of threads (FIG. 2-3; paragraph 25; 35-37) , at least one of said plurality of threads having control logic (304; FIG. 3; paragraph 23; where the thread creation monitor coupled with the logical clock analyzer is the control logic) for controlling operation of at least one other thread of said plurality of threads (FIG. 7; paragraph 35-37); and

a second configured portion within said integrated circuit for connecting said at least one thread and said at least one other thread (106, FIG. 1; 206, FIG. 2; paragraph 21; 25; 41).

13. Ma does not explicitly teach using thread circuits .

14. Nishida teaches generating thread circuits coupled with control logic (abstract; col. 6, lines 23-40).

15. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ma's invention with Nishda's to provide thread circuits for concurrently processing messages. One would have been motivated to generate thread circuits as components of the integrated circuit of Ma's system in order reduce competition among a plurality of thread operating in parallel/concurrently to access common memory (Nishida's; col. 6, lines 63-67 and col. 7, lines 1-5). Therefore to reduce cost.

16. As to claim 7, Ma teaches the invention substantially as claimed including a method of implementing multithread processing of messages (abstract) using an integrated circuit (110, FIG. 1; paragraph 15), comprising:

specifying a plurality of threads (FIG. 2; paragraph 21; 24-25) for concurrently processing messages, at least one thread of said plurality of threads including control logic (304; FIG. 3, paragraph 23) for controlling operation of at least one other thread of said plurality of threads;

specifying an interconnection topology (206; FIG. 2; 106, FIG.1; paragraph 21-22) amongst said plurality of threads, at least a portion of said interconnection topology

including a connection between said at least one thread and said at least one other thread (paragraph 25; inter threads communication) .

17. Ma does not explicitly teach generating a physical description defined in terms of component of the integrated circuit.

18. Nishida teaches generating thread circuits coupled with control logic; physical description (abstract; col. 6, lines 23-40).

19. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Ma's invention with Nishda's to provide thread circuits for message processing. One would have been motivated to generate thread circuits as components of the integrated circuit of Ma's system in order reduce competition among a plurality of thread operating in parallel to access common memory (Nishida's; col. 6, lines 63-67 and col. 7, lines 1-5). Therefore to reduce cost.

20. As to claim 8, Nishida teaches to generate data for configuring said integrated circuit with said multithreading system (abstract).

21. As to claim 11, Ma teaches, wherein said interconnection topology further comprises a second connection for communicating data from a first thread of said plurality of threads to a second thread of said plurality of threads (paragraph 22; 24-25;).

22. As to claim 12, Ma teaches, wherein said data is communicated in accordance with a data validity flag (paragraph 14).

23. As to claim 13, Ma teaches , wherein said data is communicated in *accordance* with a request generated by said second thread (paragraph 41).

24. As to claim 1 it is rejected for the same reasons as claim 7 above.

25. As to claim 2, Nishida teaches, wherein each of said plurality of thread circuits comprises a state machine (col. 6, lines 55-60).

26. As to claim 5, Ma teaches, wherein said control data comprises status data associated with said at least one other thread circuit of said plurality of thread circuits (abstract; where “checking data location” meets the claimed limitation of the claim)

27. As to claim 6, it is rejected for the same reasons as claim 7 above.

28. As to claim 14-15, they are rejected for the same reasons as claim 7 above.

29. As to claim 16, it is rejected for the same reasons as claim 2 above.

30. Claims 3-4, 9-10, 17 and 19-20, are rejected under 35 U.S.C. 103 (a) as unpatentable over Ma (US 20050038806) in view of Nishida et al. (US 6704914), as applied to claims 1-2,7-8, 14-16 and 18 above, and further in view of Rodgers et al. (US 20030126186).

31. As to claim 9-10 and 17, Ma and Nishida failed to explicitly teach a hardware description language description , a programmable logic, and a control logic configured of starting, stopping, and suspending said threads .

32. Rodgers discloses a circuit design model using a programmable logic and a hardware description language (paragraph 70-72), and a control mechanism of starting, stopping, and suspending threads (FIG. 2-3; paragraph 28, 32-33; 50).

33. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Ma, Nishida and Rodgers because the hardware description language , programmable logic coupled with the control

mechanism of starting, stopping, and suspending threads from Rodgers will improve the efficiency of Ma, Nishida 's system by allowing more efficient programming design of integrated circuits in order to allow programmers to more efficiently harness the resources of a multi-threaded processor (Rodgers's, paragraph 7).

34. As to claim 4; they are rejected for the same reasons as claim 10 above.

35. As to claims 3 and 19, they are rejected for the same reasons as claim 17 above.

36. As to claim 20, it is rejected for the same reasons as claim 2 above.

Conclusion.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdou Karim Seye whose telephone number is 571-270-1062. The examiner can normally be reached on Monday - Friday 8:30 - 6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, An Meng can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Abdou Karim Seye/
Examiner, Art Unit 2194

/Li B. Zhen/
Primary Examiner, Art Unit 2194